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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,939	08/08/2006	Jose De Jesus Pineda de Gyvez	NL04 0189 US1	9738

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EXAMINER	
JOHNSON, RYAN	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
12/13/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

PH

Office Action Summary	Application No.	Applicant(s)	
	10/588,939	PINEDA DE GYVEZ ET AL.	
	Examiner	Art Unit	
	Ryan J. Johnson	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-18* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 August 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/8/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *NPL document*.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: The specification lacks any headings between sections. The examiner recommends placing the headings "Background of the Invention", "Summary of the Invention", "Brief Description of the Drawings", and "Detailed Description of Preferred Embodiments" before their respective sections.

Appropriate correction is required.

Claim Objections

4. Claims 3,6,7,14,17 and 18 are objected to because of the following informalities: Claims 3 and 14 lack antecedent basis for the term "said feedback input". Claims 6,7,17 and 18 lack antecedent basis for the term "the periodic signal generator". The applicant underlined "according to one of claims 1 to 6", implying that said underlined term was to be added. However, said term was already present in the claim. The examiner assumes that this phrase was meant to be struck through and deleted, replacing it with the underlined phrase "according to claim 1". Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-7 and 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dalmia et al. ("Power Supply Current Monitoring Techniques for Testing PLLs", hereinafter Dalmia) in view of Somayajula et al. ("Analog Fault Diagnosis Based on Ramping Power Supply Current Signature Clusters", as cited by applicant and hereinafter Somayajula).

7. Regarding claims 1,5,9,10 and 16, Dalmia discloses a test method and apparatus for a phase locked loop (abstract) with a power supply input (power supply current), comprising a means for disabling a feedback signal to the phase comparator of the phase locked loop such that said phase locked loop is operated in an open loop

mode (during the non-operating test, the VCO is directly controlled, thus the phase comparator is disabled and the VCO operates in an open loop configuration; See pg. 369, section C), and a meter for measuring a measurement signal of the phase locked loop (Since Idd is monitored, a meter for monitoring Idd must inherently be present; see Pg. 368, section B, 1st paragraph and Pg. 369, section C). Dalmia does not explicitly disclose varying the power supply signal in such a way that the oscillator is prevented from outputting an oscillating output signal. Somayajula discloses varying the power supply in a similar current measurement testing structure (abstract, Figs.1,4) in a periodic manner (see Fig.4). Somayajula discloses that by varying the power supply voltage, fault measurements can be made while the transistors are in their various modes of operation (abstract, Pg.703, section I, 4th paragraph). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a varying power supply signal, as disclosed by Somayajula, as the power supply in the testing structure of Dalmia in order to have provided the benefits of testing for faults while transistors are in all of their operating modes. Adjusting the frequency of the power supply signal to a value in which the oscillator is prevented from outputting an oscillation signal is obvious because merely optimizing the frequency of a waveform requires only routine skill in the art.

8. Regarding claims 2 and 13, Dalmia discloses a typical PLL with a reference square wave input (Fig.1). It is well known in the art to provide a reference frequency and output frequency which alternates between Vdd and ground. Therefore, during every alternating pulse of the waveform, the reference waveform, in addition to the

feedback waveform via the VCO (Fig.5), will alternately be coupled to ground, then Vdd.

9. Regarding claims 3 and 14, Dalmia discloses that a periodic signal generator (reference input; Fig.1) is provided to both the reference input and the feedback input (via PFD, charge pump, loop filter, and VCO). When the PLL is in locked state, both the reference frequency and the VCO output will be of the same frequency, according to the inherent functionality of a PLL.

10. Regarding claims 4 and 15, Dalmia discloses measuring the current provided to the power supply input (see Pg. 368, section B, 1st paragraph and Pg. 369, section C).

11. Claims 6,7,11,12,17, and 18 are obvious because merely optimizing the frequency, thus the period, rise times and fall times, of a waveform requires only routine skill in the art.

Allowable Subject Matter

12. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: A high-pass filter and an integrator, in the context of the claims, could not be found in prior art.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Allen, III et al. (U.S. Patent No. 7,023,230) discloses testing IDD at multiple voltages.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J. Johnson whose telephone number is 571-270-1264. The examiner can normally be reached on Monday - Thursday, 9:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RJJ/

BENNY T. LEE
PRIMARY EXAMINER
ART UNIT 2817